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Optimizing Control Factors for Threshold Voltage and Leakage Current in 32 nm PMOS Transistors with the Taguchi Method

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***Abstract*—**This study utilizes the Taguchi method to optimize control factors for achieving optimal response characteristics, specifically focusing on the threshold voltage (V_{th}) and leakage current (Ileak) of a PMOS transistor with a gate length of 32 nm. The PMOS transistor design incorporates a high permittivity material (high-k) as the dielectric layer and metal gate materials such as Titanium Dioxide (T_{iO2}) and Tungsten Silicide (W_{SiX}). The optimization of control factors in PMOS device design is conducted using the Taguchi Orthogonal Array Method, with Signal-to-Noise Ratio (SNR) analysis employing Nominal-the-Best (NTB) SNR for Vth and Smaller-the-Better (STB) SNR for Ileak. Four manufacturing control factors and two noise factors are considered to optimize response characteristics and identify the optimal design parameter combination. The analysis reveals that the Halo implantation tilting angle exerts the most significant influence, with a 55.52% effect on the SNR of Ileak. The study demonstrates that Vth values exhibit minimal variance, with a mean value approximately 0.289 V ± 12.7%, while Ileak remains below 100 nA/µm, aligning with projections outlined in the International Technology Roadmap for Semiconductors (ITRS)

***Keywords: Index Terms*—32 nm PMOS T_{iO2}/W_{Six}; high-k/metal gate; threshold voltage; leakage current; Taguchi method.**

I. INTRODUCTION

Incorporating advancements in research and development within the field of complementary metal-oxide-semiconductor (CMOS) technology has significantly propelled semiconductor technology growth. While silicon dioxide (S_{iO2}) served as a reliable gate dielectric layer for many years, the downscaling of CMOS dimensions into the nanoscale range has led to reductions in gate length and changes in the thickness of the SiO2 gate layer. These alterations can introduce various challenges in CMOS characteristics, such as an increase in gate leakage current that can trigger short channel effects (SCEs) [1]. Consequently, many researchers have started transitioning to high permittivity (high-k) dielectrics as substitutes for SiO2 in CMOS gate structures due to their superior advantages [1, 2]. The International Roadmap for Semiconductor Technology (ITRS) offers valuable insights into device characteristics, serving as a resource for researchers aiming to scale down MOSFET dimensions.

Previously, our research successfully focused on analyzing control factors impacting the threshold voltage (Vth) of a 32 nm gate length PMOS device, acknowledging Vth as a critical parameter influencing CMOS device functionality [3]. This paper extends this work by employing the Taguchi

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Method to investigate both Vth and leakage current (I_{leak}) of the device. Given the significance of Vth and Ileak as key physical parameters, various techniques can be employed to optimize the device's profile and characteristics by adjusting fabrication parameters [4]. Vth represents the minimum gate voltage required to establish a channel between the source and drain. As CMOS devices shrink, the channel length between the source and drain decreases, increasing the likelihood of current leakage through the inactive transistor. To enhance Vth, it is essential to minimize Ileak to maximize device performance [5]. Each method aimed at reducing Ileak may potentially induce short channel effects, emphasizing the need for meticulous device scaling to achieve optimal performance.

This paper delves into the optimization of control factors for a PMOS transistor using the L9 Taguchi method, which leverages an orthogonal array to assess all control factors through a limited number of experiments [6]. The methodology involves Signal-to-Noise Ratio (SNR) for analyzing experimental data to identify the most effective parameter combinations efficiently [7]. The experiment incorporates two SNR metrics, namely SNR (NTB) and SNR (STB). SNR (NTB) is utilized to optimize control factors to closely align with a predetermined target or nominal value, focusing on Vth optimization. On the other hand, SNR (STB) is employed to minimize or reduce values effectively, with a particular emphasis on I_{leak}. The primary aim of this research is to conform to the ITRS projections for a 32 nm gate length PMOS transistor, targeting a Vth value of approximately 0.289V ± 12.7% and minimizing Ileak to below 100 nA/μm [10].

II. Materials and Methods

A. Fabrication using TCAD Simulation Tools

PMOS device was virtually designed with the ATHENA module. The sample was initiated by the production of a P-well based wafer with the dose of boron ions for $3.75x10^{12}$. The next step was to produce a thickness of 130 Å Shallow Trench Insulator (STI) consist of Boron Difluoride (BF_2) that functioned as the threshold-adjustment implantation. The TiO_2 was then deposited as the high-k material with 2 nm thickness followed by an etching process to produce a gate length of 32 nm. W_{Six} which is the metal gate material in this research was produced to form metal gate structure [8].

Then, the device was annealed at a temperature of 850 °C while Halo implantation was carried out to obtain optimum performance which indium is implanted with a dose of $20.45x10^{12}$ ions / cm^2 and 35°

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tilting angle and was varied to obtain the best target value. Spacer structure which located at source and drain regions is then formed. The source-drain implantation process with doses of arsenic and phosphorus ion took place. The following process has been the development of the Borophospho silicate glass layer (BPSG). Then, the wafer was being annealed for 850 °C. The process of compensation implantation by phosphorus dose in order to improve electrical profile was then took place.

To complete the device structure, the metal gate contact is formed by the aluminum layer. At this stage, the simulation design of the 32 nm PMOS device is completed, as illustrated in Figure 1 and Figure 2 which shows the list of material and the doping profile of the device respectively. Finally, the transistor went through to the analysis process on the electrical characteristics using ATLAS simulation tools in term of V_{th} and I_{leak} with referring to the prediction of ITRS.

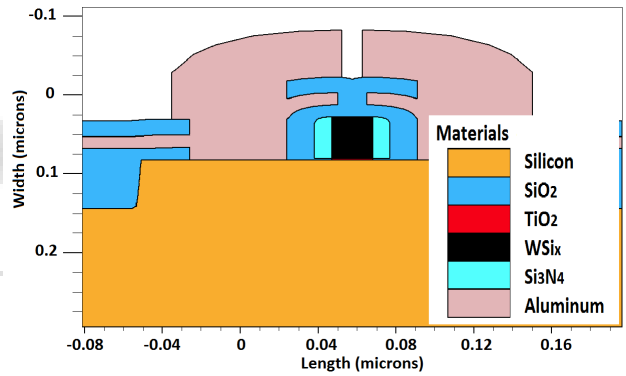

Figure 1: The PMOS transistor with TiO_2/WSi_x gate structure

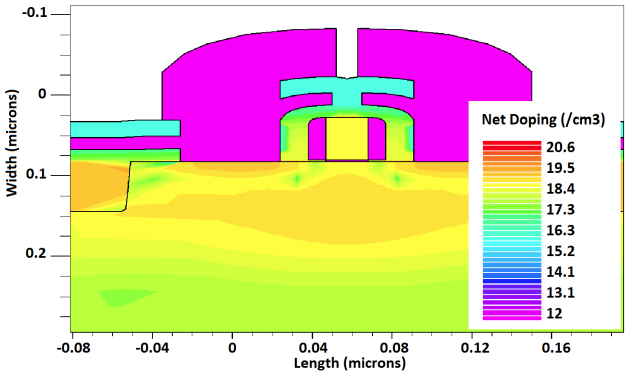

Figure 2: The doping profile of the PMOS transistor

B. The L_9 Taguchi Orthogonal Array Method

The optimizations of the PMOS device can be successful implemented by changing control factor individual. The list of all control factors and noise factors with their levels that involved in the

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experiment are listed in Table 1 and Table 2 respectively. The L_9 Taguchi orthogonal array experimental layout can be refers to [11].

Table 1
Control Factors

Factor	Control Factor	Unit	Level 1	Level 2	Level 3
A	Halo Implantation Dose (10^{12})	Atom/cm^3	20.40 (A_1)	20.45 (A_2)	20.50 (A_3)
B	Halo Implantation Tilting Angle	Degree	33 (B_1)	35 (B_2)	37 (B_3)
C	Oxide Growth Annealing Temperature	°C	808 (C_1)	810 (C_2)	812 (C_3)
D	Metal Gate Annealing Temperature	°C	848 (D_1)	850 (D_2)	852 (D_3)

Table 2
Noise Factors

Factor	Noise Factor	Unit	Level 1	Level 2
X	PSG Annealing Temperature	°C	900 (X_1)	902 (X_2)
Y	BPSG Annealing Temperature	°C	850 (Y_1)	852 (Y_2)

III. Result and Discussion

The control factors were optimized using Taguchi Method and best design will be predicted and verified. The results of V_{th} and I_{leak} obtained were analyzed in order to determine the optimum control factors for the device.

A. Electrical Characteristics of PMOS Transistor

The electrical characteristic of the designed PMOS transistor is shown in Figure 3 and Figure 4 respectively. Figure 3 shows the graph of Id versus Vd and Figure 4 shows the graph of Id versus Vg.

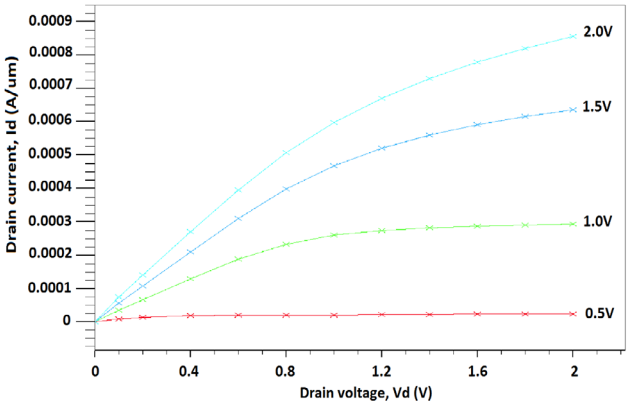

Figure 3: Id versus Vd

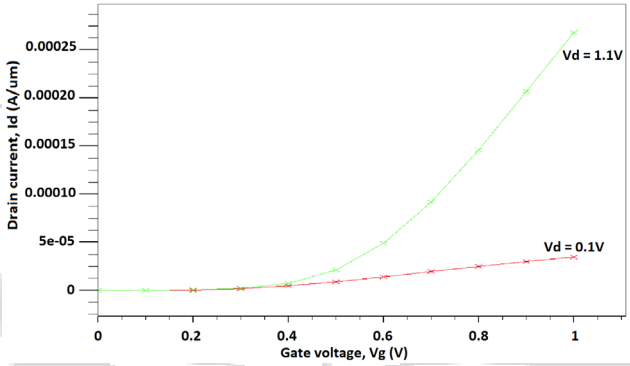

Figure 4: Id versus Vg

B. V_{th} and I_{leak} Analysis using Taguchi Method

The L_9 Taguchi method analysis for V_{th} and I_{leak} in this experiment consist of a total 36 simulation runs respectively. The completed simulation results for both V_{th} and I_{leak} are shown in Table 3 and Table 4 respectively.

Table 3
V_{th} Value for PMOS Device

Exp.	Threshold Voltage (Volts)			
	X_1Y_1	X_1Y_2	X_2Y_1	X_2Y_2
1	0.27584	0.27452	0.27594	0.27462
2	0.24246	0.24132	0.24249	0.24133
3	0.30813	0.30713	0.30855	0.30756
4	0.23408	0.23341	0.23409	0.23343
5	0.28755	0.28620	0.28801	0.28666
6	0.43549	0.43380	0.43568	0.43399
7	0.33013	0.32890	0.33080	0.32958
8	0.30311	0.30185	0.30320	0.30193
9	0.40376	0.40229	0.40380	0.40233

Table 4
I_{leak} Values for PMOS Device

Exp.	Leakage Current (nA/μm)			
	X_1Y_1	X_1Y_2	X_2Y_1	X_2Y_2
1	3.74140	3.78127	3.73861	3.77841
2	5.08231	5.13054	5.08083	5.12903
3	2.72900	2.75393	2.71674	2.74158
4	5.97259	6.03354	5.97091	6.03182
5	3.27597	3.31484	3.26188	3.30061
6	0.96864	0.97895	0.96759	0.97788
7	2.21109	2.22659	2.20086	2.21631
8	2.76319	2.79723	2.76131	2.7953
9	1.24103	1.25096	1.24068	1.2506

After completed the experiment, the next step was to analyze the control factors that give the most contribution on the device characteristics. One of the processes is to determine the SNR analysis of the experiment. As mention before, the V_{th} analysis in this experiment is referred to SNR (NTB) where the aim of the analysis is to discover the level of control factors that gives the final result value with closely or same to a target value. In this case, the target value for V_{th} is 0.289V. While for the I_{leak} analysis, the SNR of Smaller-the-Better (STB) is best uses where in the best device performance practice, the better device is the device with less I_{leak} and the best device is 100% performed with zero I_{leak}. But on a real device, that is impossible to achieve zero I_{leak}. Therefore there has limitation value for the working device where the maximum accepted of I_{leak} value is 100 nA/μm.

For The SNR (NTB), η_{NTB} can be expressed as [11]:

$$\eta_{NTB} = 10Log_{10}\left[\frac{\mu^2}{\sigma^2}\right] \quad (1)$$

where: μ_{NTB} = the mean

σ_{NTB} = the variance.

While the I_{leak} of the device is optimized using SNR (STB), η_{STB} can be expressed as:

$$\eta_{STB} = -10Log_{10}\left[\frac{1}{n}\sum_{i=1}^{n} y_i^{\,2}\right] \quad (2)$$

where: n = number of tests

Y_i = the experimental value of the I_{leak}.

By applying the formula given in Eq. (1) and Eq. (2), the η_{STB} and η_{NTB} were calculated and given as in Table 5.

In the SNR analysis, the best performance of control factor combinations is indicating by the experiment that resulted with higher SNR value. Referring to Table 5, the SNR analysis for V_{th} value shows that row 3 and row 4 gives the highest SNR values of 53.87 dB and 55.71 dB respectively. While for I_{leak}, the highest SNR values of 180.24 dB and 178.09 dB were obtained for row 6 and row 9 respectively. These values indicate that the control factor combinations give the best insensitivity for the response characteristics. As reminder, for the orthogonal experiment, the effect of each control factor on the SNR at each experiment can be separated out. The SNR for each level of the control factors is summarized in Table 6 and Table 7 both for the V_{th} and the I_{leak}.

C. Analysis of Variance (ANOVA)

In the Analysis of Variance (ANOVA), the priority of the control factors with respect to the V_{th} and I_{leak} were examined to define the accuracy of the optimum combinations. It also can be used to investigate the percentage of contribution in the performance characteristics influenced by control factors. The result of ANOVA for SNR (NTB) and SNR (STB) can be obtained in Table 8. The percentage of factor effect on SNR indicates the priority of a control factor to minimize variation. The high percentage of a factor effect on both characteristics means it has the most influence on the stability of the device [5, 12].

Based on Table 8, it shows that for Factor A which is Halo implantation dose, the factor effect percentage for I_{leak} is higher (21.50%) than that obtained for the V_{th} (8.97%) analysis. While the Halo implantation tilting angle (Factor B) has the greatest effect on the I_{leak} with 55.52% compared to the V_{th} (32.75%) and can be considered as the dominant factor. Factor C (oxide growth annealing temperature) affects the V_{th} with a value of 17.41% more than the I_{leak} (10.15%). Last but not least, for the Factor D (metal gate annealing temperature), the control factor influenced more in V_{th} compare to I_{leak}. Therefore, referring to Table 6 and Table 7, the level values with the highest SNR are selected to be the best settings for the 32 nm PMOS device which is A_3 B_2 C_2 D_3. Their best setting of control factor values is shown in Table 9.

Table 5

SNR Analysis

Exp	SNR (dB)

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No.	Threshold Voltage	Leakage Current
1	51.12	168.50
2	51.27	165.84
3	53.87	171.26
4	55.71	164.43
5	50.86	169.66
6	52.92	180.24
7	52.21	173.10
8	52.31	171.12
9	53.54	178.09

Table 6
SNR (NTB) for V_{TH}

Factor	SNR NTB (Mean), dB		
	Level 1	Level 2	Level 3
A	52.09	53.17	52.69
B	53.01	51.48	53.44
C	52.12	53.51	52.31
D	51.84	52.14	53.97

Table 7
SNR (STB) for I_{LEAK}

Factor	SNR STB (Mean), dB		
	Level 1	Level 2	Level 3
A	168.53	171.44	174.10
B	168.68	176.53	168.87
C	173.28	169.45	171.34
D	172.08	173.06	168.94

Table 8
Result of ANOVA

Factor	Factor Effect on SNR (NTB) (%)	Factor Effect on SNR (STB) (%)
A	8.97	21.50
B	32.75	55.52
C	17.41	10.15
D	40.87	12.83

Table 9
Best Setting of the Control Factors

Factor	Level	Best Value
A	3	$20.5x10^{12}$
B	2	35
C	2	810
D	3	852

Table 10
Final Simulation with Added Noise

Noise (°C)	V_{th} (V)	I_{leak} (nA/μm)
(X_1,Y_1)	0.30266	2.77693
(X_1,Y_2)	0.30140	2.81094
(X_2,Y_1)	0.30271	2.77537
(X_2,Y_2)	0.30144	2.80936

These final control factors were then simulated with different parametric values of the noise factors to get the optimal result of V_{th} and I_{leak} as noted in Table 10. Finally, the control factor combination of A_3 B_2 C_2 D_3 X_1 Y_2 shows the best combination where the V_{th} value of 0.3014V resulted the closest value to the ITRS prediction by 4.29% (ITRS range: ±12.7%), and in the same time I_{leak} resulted with almost 97% away and lower from maximum value as predicted from ITRS. Well said, both these values are in line with the ITRS predictions. As a result, Taguchi Method is proven to be a capable method to predict the optimum solution in obtaining the optimal fabrication recipe for a 32 nm TiO_2/WSi_x planar PMOS with compliant V_{th} and I_{leak} values.

IV. Conclusion

As a conclusion, the best fabrication control factor settings for a 32nm TiO_2/WSi_x planar PMOS transistor using Taguchi method was successfully achieved. The Halo tilting angle has been identified to be the dominant factor in determining the value of both the V_{th} and the I_{leak}. The parametric combination of the process factors which include noise factors have resulted in the successful development of the nanoscale PMOS device with the combination of control factor A_3 B_2 C_2 D_3 X_1 Y_2 was the best combination in order to achieve the best V_{th} which closest to the nominal value and minimum I_{leak} where these values comply with the specifications given in ITRS and these values also reported by another researcher [11, 12].

Our future work involves developing the device using more fabrication's process parameters. We will also optimize both the V_{th} and the turn-on/turn-off current for the 32nm gate length PMOS device using extended Taguchi's method in the future.

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